

SPS-9380V-2RG

(RoHS Compliant)

1260 to 1620 nm / 3 Gb/s Dual Optical SM Receiver

FEATURES

- I SMPTE 297-2006 Compliant
- I Speed from 50 Mbps to 3Gbps
- I Support Video Pathological Patterns for SD-SDI, HD-SDI and 3G-SDI
- I Dual High Sensitivity APD Receiver with Duplex LC
- I Based on Industry Standard SFP
- I Single +3.3 V Power Supply
- I RoHS Compliant
- I 0 to 70°C Operation
- I Hot Pluggable

DESCRIPTION

The SPS-9380V-2RG is a dual channel optical single mode receiver module designed to receive optical serial digital signals as defined in SMPTE 297-2006. It supports from 50 Mbps to 3 Gbps and is specifically designed for received the SMPTE 259M, SMPTE 344M, SMPTE 292M and SMPTE 424M SDI pathological patterns. It is with the SFP 20-pin connector to allow hot plug capability. Each receiver can receive signal from 50 Mbps to 3 Gbps with up to 30 km of single-mode fiber when using the SPS-9380V-2TG as the transmitter. A maximum distance of 80 km is achievable with 3Gbps pathological signals.

APPLICATIONS

- I SMPTE 297-2006 Compliant Electrical-to-Optical Interfaces
- I High-density Video Routers

ORDER INFORMATION

P/No.	Type	Bit Rate (Mb/s)	RX1		RX2		Package	Temp (°C)	RoHS Compliant
			λ (nm)	Sen. (dBm)	λ (nm)	Sen. (dBm)			
SPS-9380V-2RG	2-RX	50 to 3000	1260/1620	-9 to -28	1260/1620	-9 to -28	LC SFP	0 to 70	Yes

ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute Maximum Ratings					
Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	Tstg	-40	85	°C	
Operating Case Temperature	Tc	0	70	°C	
Power Supply Voltage	Vcc	0	4	V	
ESD Tolerance on all pins			1	KV HBM	
Relative Humidity	---	5	95	% RH	non-condensing

Recommended Operating Conditions					
Parameter	Symbol	Min	Typ	Max	Units / Notes
Power Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case Temperature	Tc	0		70	°C
Baud Rate		50		3000	Mb/s
Power Supply Current	Icc		200	250	mA

Receiver Specifications (0°C < Tc < 70°C, 3.13V < Vcc < 3.47V)						
Parameter	Symbol	Min	Typ	Max	Units	Notes
Optical						
Wavelength of Operation		1260	---	1620	nm	
Sensitivity for SMPTE 424M 2.97 Gb/s	Sen	-9	---	-28	dBm	Pathological
		-9	---	-28	dBm	PRBS 2 ²³ -1, BER=1E-12
Sensitivity for SMPTE 292M 1.485 Gb/s	Sen	-9	---	-28	dBm	Pathological
		-9	---	-28	dBm	PRBS 2 ²³ -1, BER=1E-12
Signal Detect -- Asserted	Pa	---	---	-28	dBm	Transition: low to high
Signal Detect -- Deasserted	Pd	-36	---	---	dBm	Transition: high to low
Signal detect -- Hysteresis		1		6	dB	
Optical Return Loss			-27		dB	
Electrical						
CML Output (Differential)		550	660	850	mVp-p	AC coupled output
Optical Rise Time / Fall Time	tr / tf			135	ps	1, SMPTE 424M
				270	ps	1, SMPTE 292M
				800	ps	1, SMPTE 344M
				1.5	ns	1, SMPTE 259M
Output LOS Voltage -- Low	V _{OL}	0		0.5	V	I _{OL} =-1.6mA, 1 TTL unit load
Output LOS Voltage -- High	V _{OH}	2.5		Vcc+0.3	V	I _{OH} =40µA, 1 TTL unit load
SCL, SDA	V _{OH}	2.5		Vcc+0.3	V	
	V _{OL}	0		0.5	V	

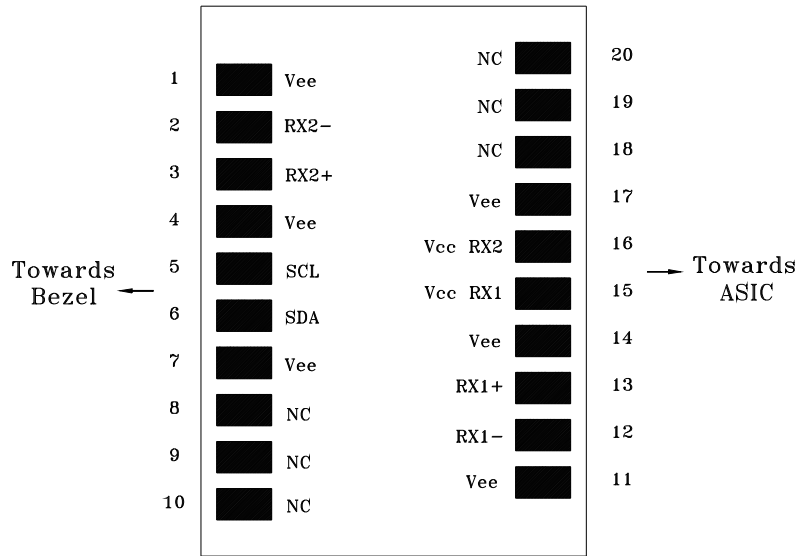
1. 20% to 80%, unfiltered.

MODULE DEFINITION

Module Definition	PIN 5	PIN 6	Interpretation by Host
4	SCL	SDA	Serial module definition protocol

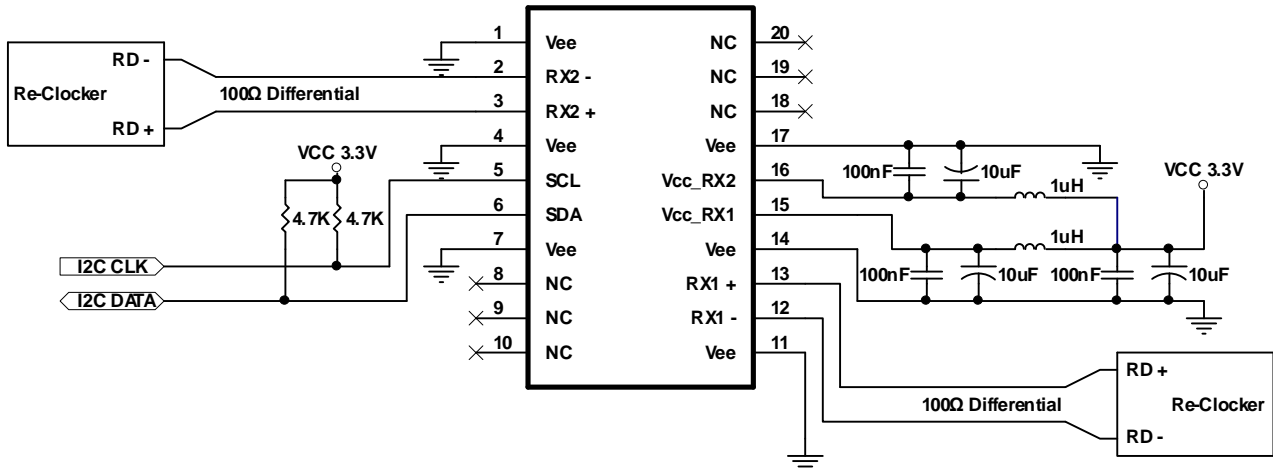
Module Definition 4 specifies a serial definition protocol. For this definition, upon power up, SCL and SDA appear as no connector (NC). When the host system detects this condition, it activates the serial protocol. The protocol uses the 2-wire serial CMOS E²PROM protocol of the ATMEL AT24C01A/02/04 family of components.

CONNECTION DIAGRAM



PIN	Name	Function	Notes
1	Vee	Signal Ground	
2	RX2-	Negative Differential Output (2)	
3	RX2+	Positive Differential Output (2)	
4	Vee	Signal Ground	
5	SCL	Serial I ² C Clock	
6	SDA	Serial I ² C Data	
7	Vee	Signal Ground	
8	NC	No Connection	
9	NC	No Connection	
10	NC	No Connection	
11	Vee	Signal Ground	
12	RX1-	Negative Differential Output (1)	
13	RX1+	Positive Differential Output (1)	
14	Vee	Signal Ground	
15	Vcc RX1	Power Supply (1)	+3.3V±5%
16	Vcc RX2	Power Supply (2)	+3.3V±5%
17	Vee	Signal Ground	
18	NC	No Connection	
19	NC	No Connection	
20	NC	No Connection	

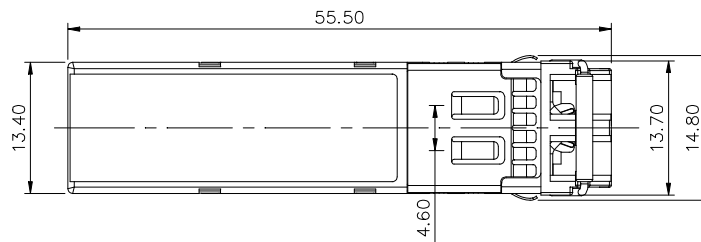
RECOMMENDED CIRCUIT SCHEMATIC



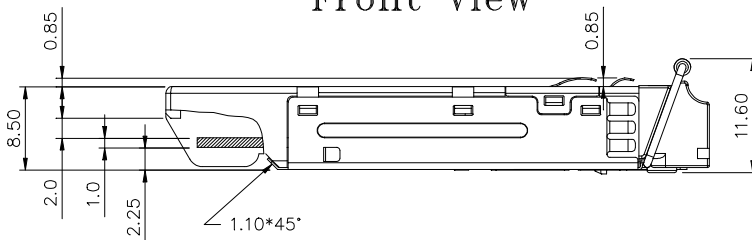
1. Consult Chipset manufacturer's data sheet and application data for appropriate receiver input biasing network.

PACKAGE DIAGRAM (Units in mm)

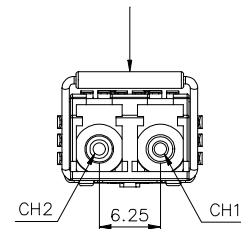
Top View



Front View

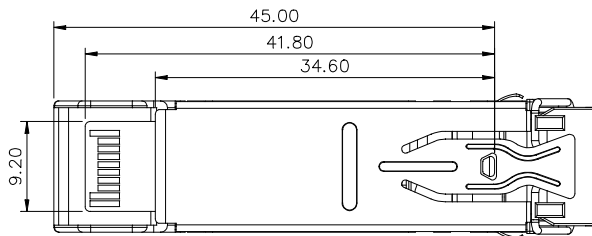


LATCH COLOR
BLUE



Side View

Bottom View



REVISION HISTORY

Version	Subject	Release Date
1.0	Initial datasheet	2009/3/1