TRSL-93120F-CXX0G

3.3V / CWDM / 2.125 Gbps SFF LC SINGLE-MODE TRANSCEIVER

FEATURES

- 18-Wavelength CWDM Transceiver
- Duplex LC Single Mode Transceiver
- Fibre Channel 2X/1X SM-LC-L FC-PI Compliant
- IEEE 802.3z Gigabit Ethernet Compliant
- Small Form Factor, RJ-45 size, 2X5 pin Package
- CWDM DFB LD Transmitter
- 30 dB Link Power Budget at Least
- AC/AC Coupled Signal Input / Output
- LVTTL Transmitter Disable Input
- LVTTL Signal Detection Output
- Single +3.3 V Power Supply
- 0 to 70°C Operation
- Wave Solderable and Aqueous Washable
- Class 1 Laser International Safety Standard IEC-60825 Compliant

APPLICATIONS

- ATM Switches and Routers
- SONET / SDH Switch Infrastructure
- XDSL Applications
- Metro Edge Switching

DESCRIPTION

The TRSL-93120F-CXX0G series single mode transceivers is small form factor, low power, high performance CWDM module for bi-directional serial optical data communications such as Fiber Channel 2X/1X SM-LC-L FC-PI and IEEE 802.3z Gigabit Ethernet 1000BASE-ZX. There are eighteen center wavelengths available from 1270 nm to 1610 nm, each step 20 nm. A guaranteed minimum optical link budget of 30 dB is offered. The transmitter section uses a multiple quantum well CWDM DFB laser and is a class 1 laser compliant according to International Safety Standard IEC-60825. The receiver section uses an integrated InGaAs detector preamplifier (IDP) mounted in an optical header and a limiting post-amplifier IC. A PECL logic interface simplifies interface to external circuitry.

LASER SAFETY

This single mode transceiver is a Class 1 laser product. It complies with IEC-60825 and FDA 21 CFR 1040.10 and 1040.11. The transceiver must be operated within the specified temperature and voltage limits. The optical ports of the module shall be terminated with an optical connector or with a dust plug.

ORDER INFORMATION

P/No.	Bit Rate (Gb/s)	FC-PI	Power Budget (dB)	Wavelength (nm)	Package	Temp. (°C)	TX Power (dBm)	RX Sens. (dBm)	RoHS Compliant
TRSL-93120F-CXX0G	2.125/1.063	200/100	> 30	CWDM*	2X5 LC	0 to 70	5 to 0	-30	Yes

CWDM Wavelength (0 to 70°C)

Central Wavelength	Min. (nm)	Typ. (nm)	Max. (nm)	Central Wavelength	Min. (nm)	Typ. (nm)	Max. (nm)
-C270	1264.5	1270	1277.5	-C450	1444.5	1450	1457.5
-C290	1284.5	1290	1297.5	-C470	1464.5	1470	1477.5
-C310	1304.5	1310	1317.5	-C490	1484.5	1490	1497.5
-C330	1324.5	1330	1337.5	-C510	1504.5	1510	1517.5
-C350	1344.5	1350	1357.5	-C530	1524.5	1530	1537.5
-C370	1364.5	1370	1377.5	-C550	1544.5	1550	1557.5
-C390	1384.5	1390	1397.5	-C570	1564.5	1570	1577.5
-C410	1404.5	1410	1417.5	-C590	1584.5	1590	1597.5
-C430	1424.5	1430	1437.5	-C610	1604.5	1610	1617.5

CWDM*: 18 Wavelengths from 1270 nm to 1610nm, each step 20 nm.

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Absolute Maximum Ratings					
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Notes**
Storage Temperature	Tstg	-40	85	°C	
Operating Temperature	Topr	0	70	°C	With air flow 1m/sec
Soldering Temperature	---		260	°C	10 seconds on leads only
Power Supply Voltage	Vcc	0	4.5	V	
Input Voltage	---	GND	Vcc	V	
Output Current	Iout	0	30	mA	

Recommended Operating Conditions					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units / Notes**
Power Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Temperature	Topr	0		70	°C / air flow 1m/sec
Data Rate		1063	2125		Mb/s
Power Supply Current	Icc		200	300	mA

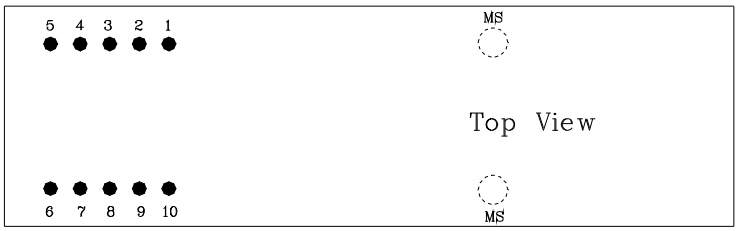
Transmitter Specifications ($0^oC < Topr < 70^oC$, $3.13V < Vcc < 3.47V$)						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes**
Optical						
Optical Transmit Power	Po	0	---	5	dBm	1
Output Center Wavelength	λ	λ-5.5	λ	λ+7.5	nm	2
Output Spectrum Width	Δλ	---	---	1	nm	-20 dB Width
Side Mode Suppression Ratio	SMSR	30			dB	
Extinction Ratio	E_R	---	9	---	dB	
Optical Rise Time	t_r			160	ps	20% to 80% Values
Optical Fall Time	t_f			160	ps	20% to 80% Values
Relative Intensity Noise	RIN			-120	dB/Hz	
Electrical						
Data Input Current – Low	I_{IL}	-350			μA	
Data Input Current – High	I_{IH}			350	μA	
Differential Input Voltage	V_{IH} - V_{IL}	300			mV	
Data Input Voltage – Low	V_{IL} - V_{CC}	-2.0		-1.58	V	3
Data Input Voltage -- High	V_{IH} - V_{CC}	-1.1		-0.74	V	3
Disable Input Voltage -- Low	$V_{TDIS,L}$	0		0.5	V	TX Output Enabled
Disable Input Voltage -- High	$V_{TDIS,H}$	Vcc – 1.3		Vcc	V	TX Output Disabled
Shut Off Time for TxDis	t_{DIS}			1	ms	

Notes: 1. Output power is power coupled into a 9/125 μm single mode fiber.
2.ITU-T G.694.2 CWDM wavelength from 1270 nm to 1610 nm, each step 20nm.
3.These inputs are compatible with 10K, 10KH and 100K ECL and PECL inputs.

Receiver Specifications (0^oC < Topr < 70^oC, 3.13V < Vcc < 3.47V)						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes**
Optical						
Sensitivity @ 2.125 Gbps	Sen. 2X	---	---	-30	dBm	1
Sensitivity @ 1.063 Gbps	Sen. 1X	---	---	-30		1
Maximum Input Power	Pin	-9		---	dBm	
Signal Detect -- Asserted	Pa	---	---	-30	dBm	Transition: low to high
Signal Detect -- Deasserted	Pd	-45	---	---	dBm	Transition: high to low
Signal detect -- Hysteresis		1.0	---		dB	
Wavelength of Operation		1100	---	1620	nm	
Electrical						
Data Output Voltage – Low	V_{OL} - V_{CC}	-2.0		-1.58	V	2
Data Output Voltage – High	V_{OH} - V_{CC}	-1.1		-0.74	V	2
Signal Detect Output Voltage -- Low	V_{OL}			0.5	V	
Signal Detect Output Voltage -- High	V_{OH}	2.0			V	

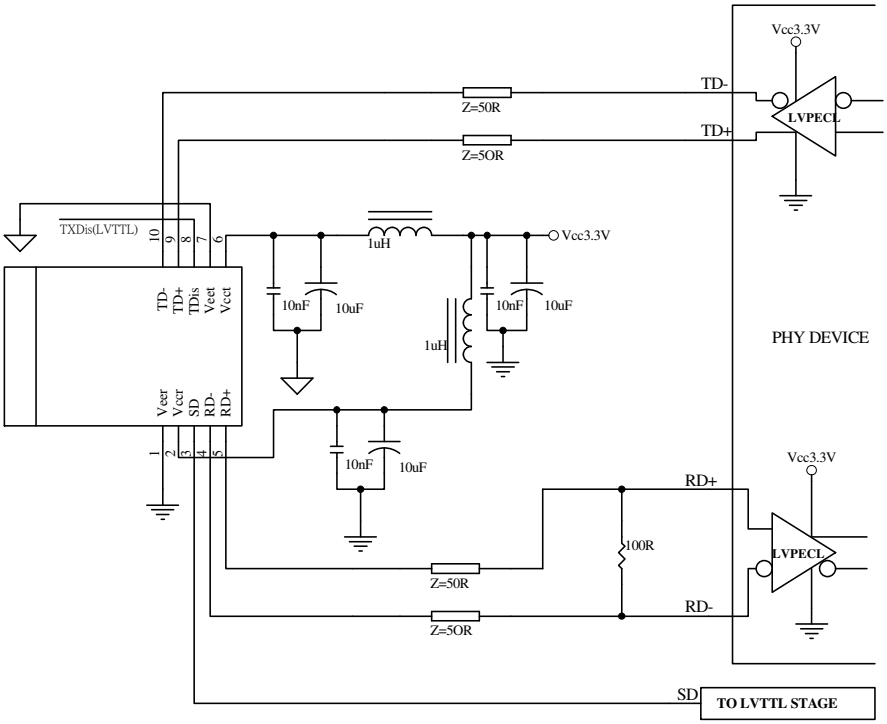
Notes: 1. Minimum sensitivity and saturation levels at BER=1E-12 for a 2^7-1 PRBS.
2.These outputs are compatible with 10K, 10KH and 100K ECL and PECL outputs.

CONNECTION DIAGRAM



PIN	Symbol	Notes
1	V_{EE}r	Directly connect this pin to the receiver ground plane
2	V_{CC}r	+3.3V dc power for the receiver section
3	SD	Active high on this indicates a received optical signal.
4	RD–	Receiver Dataout Bar. See recommended circuit schematic
5	RD+	Receiver Dataout. See recommended circuit schematic
6	V_{CC}t	+3.3V dc power for the transmitter section
7	V_{EE}t	Directly connect this plan to the transmitter ground plane
8	TDis	Transmitter Disable. Connect this pin to +3.3V TTL logic "1" to disable module To enable module connect to TTL logic low "0"
9	TD+	Transmitter Data In. See recommended circuit schematic
10	TD-	Transmitter Data In Bar. See recommended circuit schematic
MS	MS	Mounting Studs. Connect to Chassis Ground

RECOMMENDED CIRCUIT SCHEMATIC

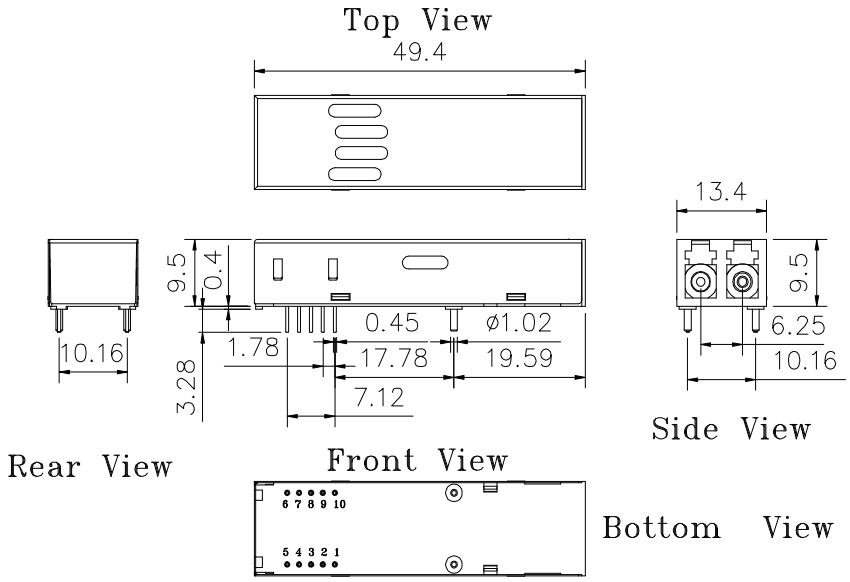


Note: 1. TX input is terminated inside the module.
2. Veer and Veet are not internally connected to each other.
3. 50 Ω line pattern and component placements on TD+/TD- and RD+/RD- lines shall be symmetrical for better impedance matching.

PACKAGE DIAGRAM

Units in mm

1) Standard Case



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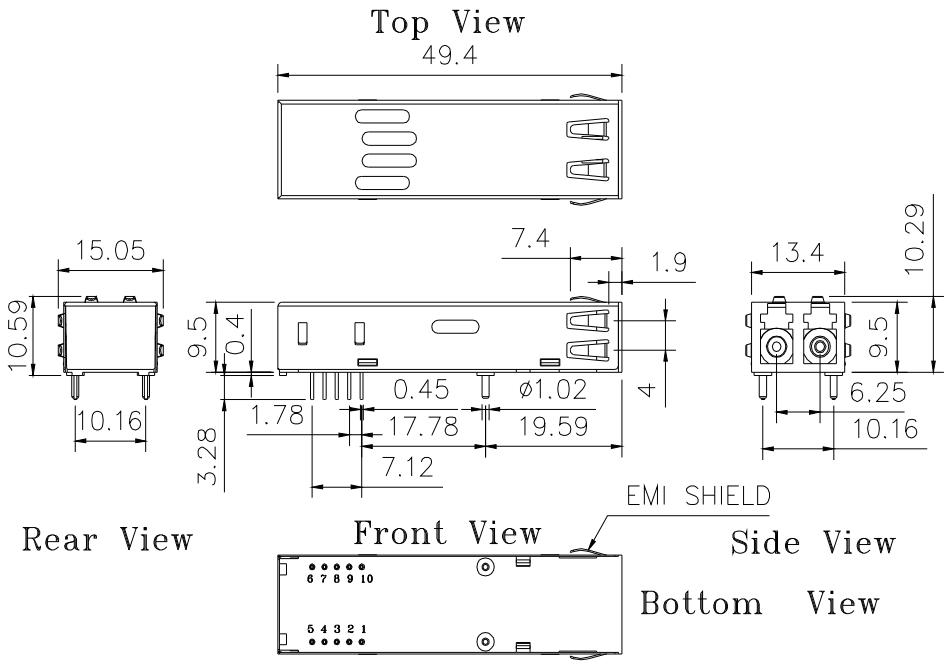
2) Extended Case



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Note: Specifications subject to change without notice.