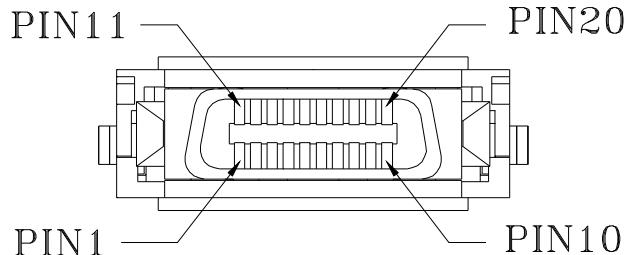


PIN ASSIGNMENT



PIN	Signal Name	Sequence	Description
1	RX-LOS	2	Receiver Loss of Signal, logic high, open collector compatible, 4.7K to 10K ohm pull-up to V _{CC} T on host
2	R _{GND}	2	Receiver Ground
3	R _{GND}	2	Receiver Ground
4	MOD-DEF(0)	2	TTL Low
5	MOD-DEF(1)	2	SCL Serial Clock Signal
6	MOD-DEF(2)	2	SDA Serial Data Signal
7	TX-DIABLE	2	Transmitter Disable, logic high, open collector compatible
8	T _{GND}	2	Transmitter Ground
9	T _{GND}	2	Transmitter Ground
10	TX-FAULT	2	Transmitter Fault, logic high, open collector compatible, 4.7K to 10K ohm pull-up to V _{CC} T on GBIC
11	R _{GND}	1	Receiver Ground
12	-RX-DAT	1	Receiver Data Bar, Differential PECL, AC coupled
13	+RX-DAT	1	Receiver Data, Differential PECL, AC coupled
14	R _{GND}	1	Receiver Ground
15	V _{CCR}	2	Receiver +5V Supply
16	V _{CC} T	2	Transmitter +5V Supply
17	T _{GND}	1	Transmitter Ground
18	+TX-DAT	1	Transmitter Data, Differential PECL, AC coupled
19	-TX-DAT	1	Transmitter Data Bar, Differential PECL, AC coupled
20	T _{GND}	1	Transmitter Ground

A sequence value of 1 indicates that the signal is in the first group to engage during plugging of a module. A sequence value of 2 indicates that the signal is the second and last group. The two guide pins on the connector are electrically connected to the transceiver circuit ground. These two guide pins make contact with circuit prior to sequence 1 signals.

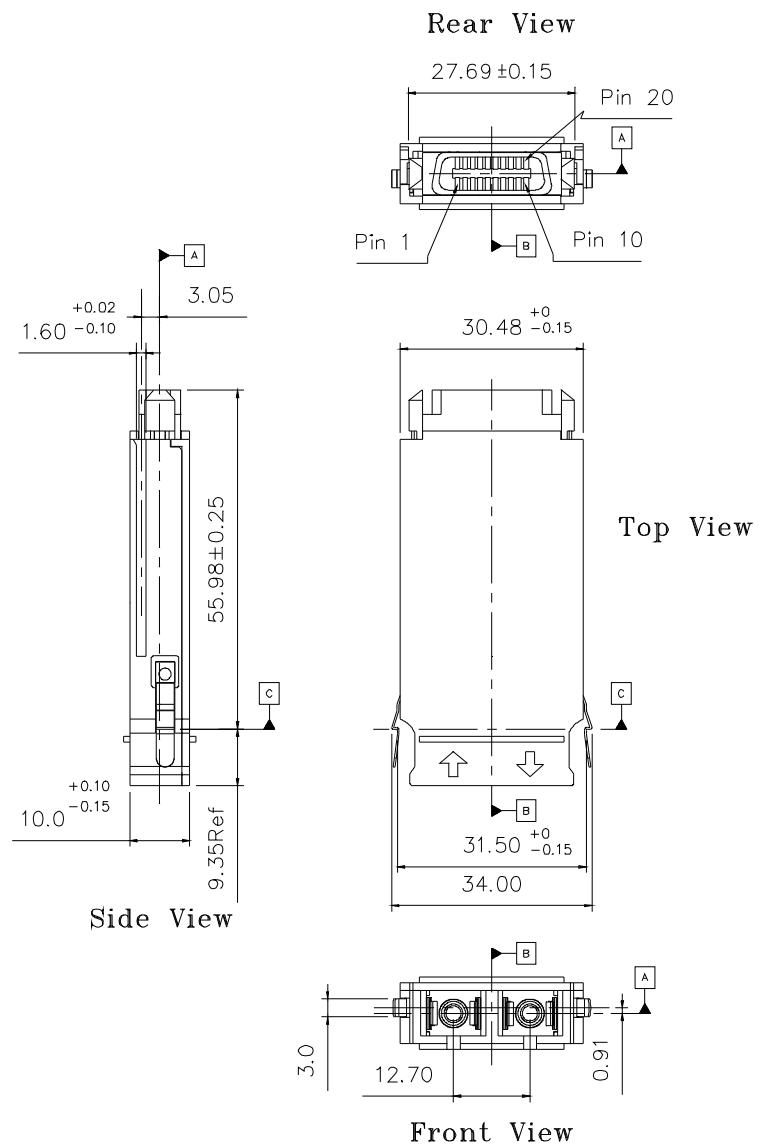
Module Definition

Module Definition	MOD-DEF(0) PIN 4	MOD-DEF (1) PIN 5	MOD-DEF (2) PIN 6	Interpretation by Host
4	TTL Low	SCL	SDA	Serial module definition protocol

Module Definition 4 specifies a serial definition protocol. For this definition, upon power up, MOD-DEF(1:2) appear as no connector (NC) and MOD-DEF(0) is TTL LOW. When the host system detects this condition, it activates the serial protocol. The protocol uses the 2-wire serial CMOS E²PROM protocol of the ATMEL AT24C01A/02/04 family of components.

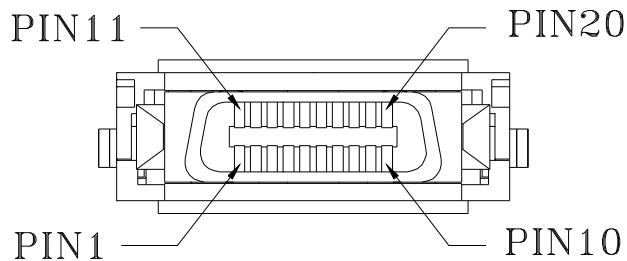
PACKAGE DIAGRAM

Units in mm



Note: Specifications subject to change without notice.

PIN ASSIGNMENT



PIN	Signal Name	Sequence	Description
1	RX-LOS	2	Receiver Loss of Signal, logic high, open collector compatible, 4.7K to 10K ohm pull-up to V_{CC} T on host
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14	R_{GND}	1	Receiver Ground
15	V_{CCR}	2	Receiver +5V Supply
16	$V_{CC}T$	2	Transmitter +5V Supply
17	T_{GND}	1	Transmitter Ground
18	+TX-DAT	1	Transmitter Data, Differential PECL, AC coupled
19	-TX-DAT	1	Transmitter Data Bar, Differential PECL, AC coupled
20	T_{GND}	1	Transmitter Ground

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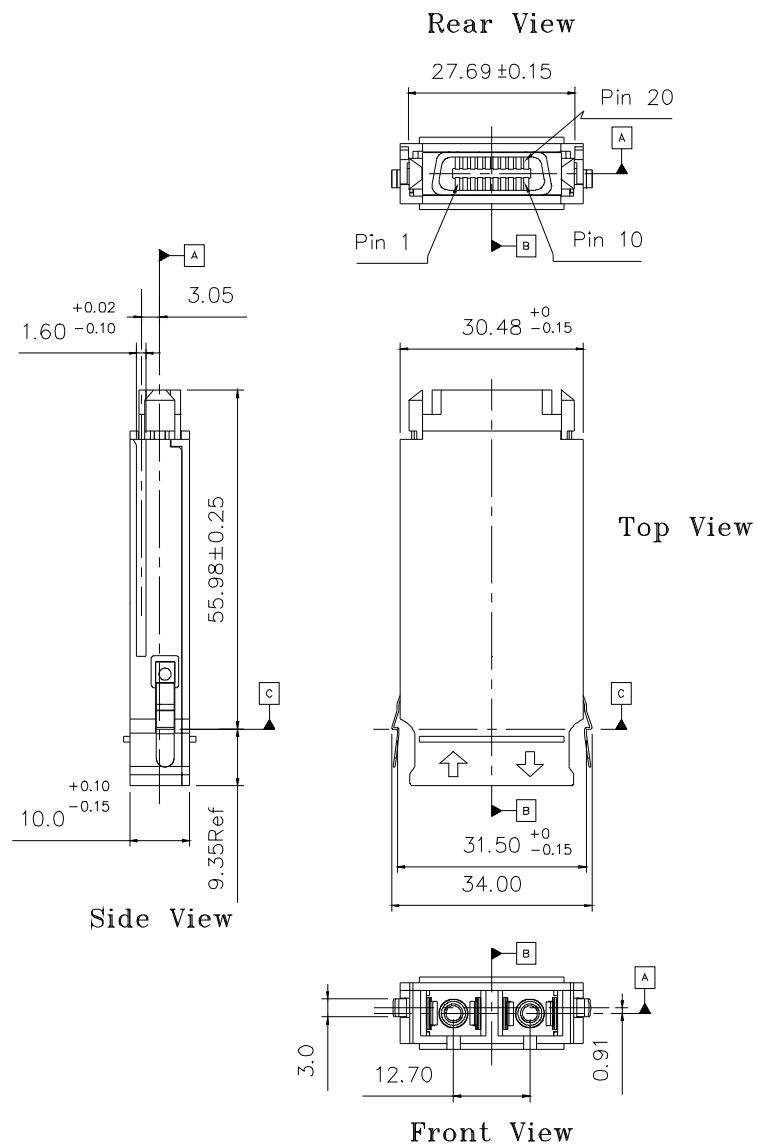
Module Definition

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PACKAGE DIAGRAM

Units in mm



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