XPB-4910LWG / XPB-4910BLWG (RoHS Compliant)

1330 nm TX / 1270 nm RX , 8.5Gbps 1-Fiber Single-Mode LC XFP Transceiver

FEATURES

- 1-Fiber Bi-Directional XFP Optical Transceiver
- Up to 8.5 Gbps Bi-directional Data Links
- Complaint with XFP MSA
- Compliant with 8G FC-BX
- Compliant with 4G and 2G Fibre Channel
- SFF-8472 Digital Diagnostic Function
- Simplex LC Connector
- 1330 nm DFB LD Transmitter
- 1270 nm Receiver
- Distance up to 10km
- 2-Wire Interface for Integrated Digital Diagnostic Monitoring
- XFI Loopback Mode
- No reference Clock required
- Only Required +3.3 V Power Supply
- Power Consumption < 2 W
- RoHS Compliant
- 0 to 70°C Operating : XPB-4910LWG
- -10 to 85°C Operating : XPB-4910BLWG

APPLICATIONS

- 8G Fibre Channel Links

LASER SAFETY

This single-mode transceiver is a Class 1 laser product. It complies with IEC-60825 and FDA 21 CFR 1040.10 and 1040.11. The transceiver must be operated within the specified temperature and voltage limits. The optical ports of the module shall be terminated with an optical connector or with a dust plug.

DESCRIPTION

XPB-4910LWG series transceivers are single-mode transceiver for bi-directional serial optical data communications such as 8x/4x/2x FC-BX by using 1330 nm transmitter and 1270 nm receiver.

The transceiver consists of two sections: The transmitter section consists of a directly modulated 1330 nm DFB laser and is a class 1 laser compliant according to International Safety Standard IEC 60825. The receiver section uses an integrated 1270nm detector preamplifier (IDP) mounted in an optical header and a limiting post-amplifier IC.

The module is with the XFP 30-pin connector to allow hot plug capability. Integrated Tx and Rx signal conditioners provide high jitter-tolerance for full XFI compliance and no external reference clock required. The internally ac coupled high speed serial I/O simplifies interfacing to external circuitry. Only single 3.3V power supply is needed. The optical output can be disabled by LVTTL logic high-level input of TX_DIS. Loss of signal (RX_LOS) output is provided to indicate the loss of an input optical signal of receiver.

A serial EEPROM in the transceiver allows the user to access transceiver digital diagnostic monitoring and configuration data via the 2-wire XFP Management Interface. This interface uses a single address, A0h, with a memory map divided into a lower and upper area. Basic digital diagnostic data is held in the lower area while specific data is held in a series of tables in the high memory area.

ORDER INFORMATION

P/No.	Bit Rate (Gb/s)	FC-PI-4	Distance (km)	TX (nm)	RX (nm)	Package	Temp (°C)	RoHS Compliant
XPB-4910LWG	8 / 4 / 2	BX	10	1330 DFB	1270	LC XFP with DMI	0 to 70	Yes
XPB-4910BLWG	8 / 4 / 2	BX	10	1330 DFB	1270	LC XFP with DMI	-10 to 85	Yes

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Absolute Maximum Ratings					
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Notes**
Storage Temperature	Tstg	-40	85	°C	
Operating Case Temperature	Topr	0 -10	70 85	°C	XPB-4910LWG XPB-4910BLWG
Relative Humidity	RH	0	85	%	Non condensing
Power Supply Voltage	$V_{CC}3$	0	3.6	V	

Recommended Operating Conditions					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units / Notes**
Power Supply Voltage	$V_{CC}3$	3.13	3.3	3.47	V
Power Supply Current (@3.3V)	$I_{CC}3$			550	mA
Power Dissipation	P_D			2	W
Operating Case Temperature	Topr	0 -10		70 85	°C / XPB-4910LWG °C / XPB-4910BLWG
Data Rate			8.5		Gb/s

Transmitter Optical Specifications (Topr= 0 to 70°C, Vcc3 = 3.3V ±5%)						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes**
Average Launch Power	$Po_{,Avg}$	-5		0	dBm	1
Output Center Wavelength	λc	1320	1330	1340	nm	
Output Spectrum Width	σ_λ			1	nm	-20 dB width
Side Mode Suppression Ratio	SMSR	30			dB	
Relative Intensity Noise	RIN			-128	dB/Hz	
Optical Eye Mask	Compliant with IEEE 802.3ae 10GBASE-L XFP MSA					
Average Launch Power of OFF Transmitter				-30	dBm	

1. Output power is power coupled into a 9/125 μm single-mode fiber.

Receiver Optical Specifications (Topr= 0 to 70°C, Vcc3 = 3.3V ±5%)						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes**
Sensitivity @ 8.5Gb/s	Sen1			-14	dBm	2, average received power
Receiver Overload	P_{MAX}	0.5	---		dBm	
LOS -- Deasserted	LOS_D	---	---	-18	dBm	Transition: low to high
LOS -- Asserted	LOS_A	-30	---	---	dBm	Transition: high to low
LOS -- Hysteresis		1	---	5	dB	
Wavelength of Operation	λc	1260		1280	nm	3

2. Measured with worst ER; BER < 10^{-12} and PRBS 2^7-1.
3. At least 30 dB optical isolation for the wavelength 1320 to 1340 nm.

Electrical Characteristics						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes**
High-Speed Signal (CML) Interface Specification						
Input Data Rate			8.5		Gb/s	
TX Clock Tolerance				±100	ppm	4
Differential Input Impedance	Rin		100		Ω	
Differential Data Input Amplitude		120		820	mVpp	5, Internally AC coupled
Output Data Rate			8.5		Gb/s	
RX Clock Tolerance				±100	ppm	4
Differential Output Impedance	Rout		100		Ω	
Differential Data Output Amplitude		340		850	mVpp	5, Internally AC coupled
Low-Speed Signal (LVTTL) Interface Specification						
Input High Voltage		2.0		Vcc	V	
Input Low Voltage		GND		0.8	V	
Output High Voltage		2.4		Vcc	V	
Output Low Voltage		GND		0.5	V	
Reference Clock (LVPECL) Interface Specification						
No reference clock						

4. Clock tolerance for 8.5Gb/s, 4.25Gb/s, 2.12Gb/s, 1.063Gb/s and 1.25Gb/s.

5. The differential input and output amplitudes are per XFP MSA mask at points B' and C'.

Transceiver Timing Characteristics						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes**
TX_DIS Assert Time	t_off			10	μs	
TX_DIS Negate Time	t_on			2	ms	
Time to Initialize	t_init			300	ms	
Interrupt Assert Delay	interrupt_on			200	ms	
Interrupt Negate Delay	interrupt_off			500	μs	
P_Down/PST Assert Delay	P_Down/RST_on			100	μs	
P_Down Nagate Delay	P_Down/RST_off			300	ms	
Mod_NR Assert Delay	Mod_nr_on			1	ms	
Mod_NR Negate Delay	Mod_nr_off			1	ms	
Mod_Desel Assert Time	T_Mod_Desel			2	ms	
Mod_Desel De-Assert Time	T_Mod_Sel			2	ms	
P_Down Reset Time	T_reset	10			μs	
RX_LOS Assert Delay	T_Los_on			100	μs	
RX_LOS Negate Delay	T_Los_off			100	μs	
Serial ID Clock Rate	f_{SCL}	0		400	kHz	

Management Interface

The structure of the memory map is shown in Figure 1, which is accessible over a 2-wire serial interface at the 8-bit address 1010000X (A0h). The normal 256 byte I2C address space is divided into low and upper blocks of 128 Bytes. The lower block of 128 Bytes is always directly available and is used for the diagnostics and control function. Multiple blocks of memories are available in the upper 128 Bytes of the address space. These are individually addressed through a table select Byte which the user enters into a location in the lower address space. Thus, there is a total available address space of 128*256 = 32 Kbytes in this upper memory space. The contents of Table 01h are listed in Table 1 below. Please refer SFF INF-8077i (Revision 4.5) for detailed information.

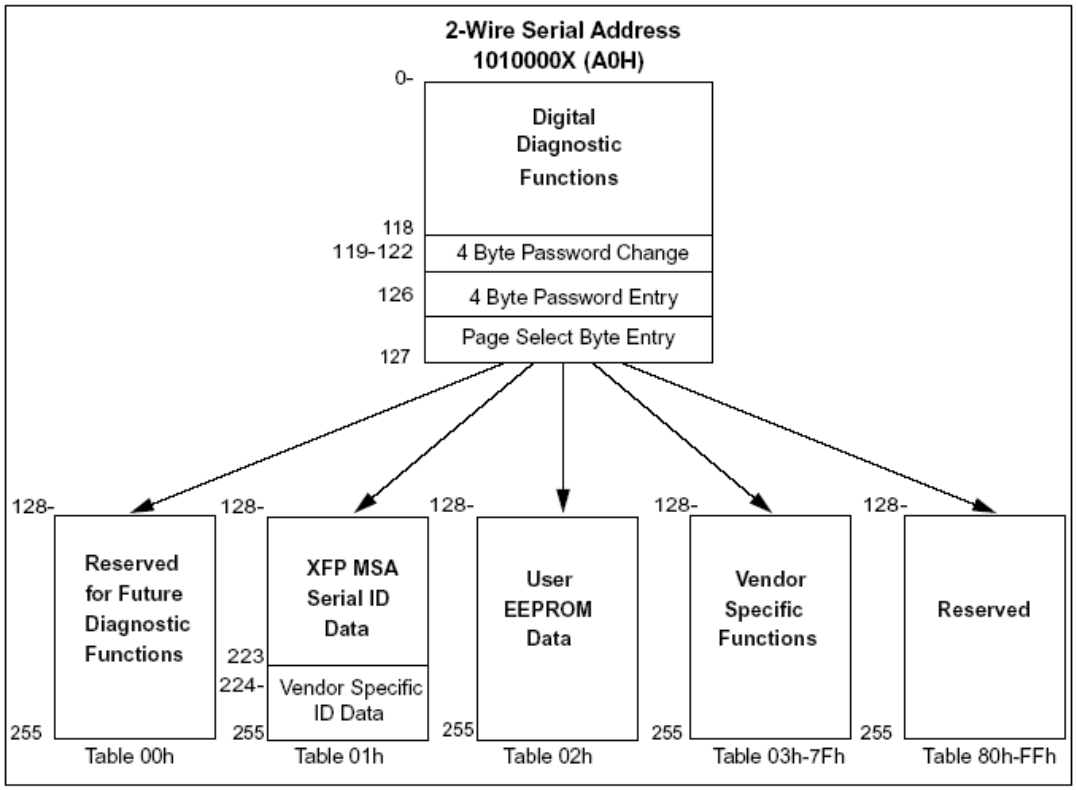


Figure 1. 2-wire Serial Digital Diagnostic Memory Map

Table 1 Monitoring Specification

Data Address	Parameter	Accuracy
96 ~ 97	Temperature	± 3°C
98 ~ 99	Reserved	
100 ~ 101	Tx Bias	± 10%
102 ~ 103	Tx Power	± 2dB
104 ~ 105	Rx Power	± 2dB
106 ~ 107	Vcc3	± 3%

CONNECTION DIAGRAM

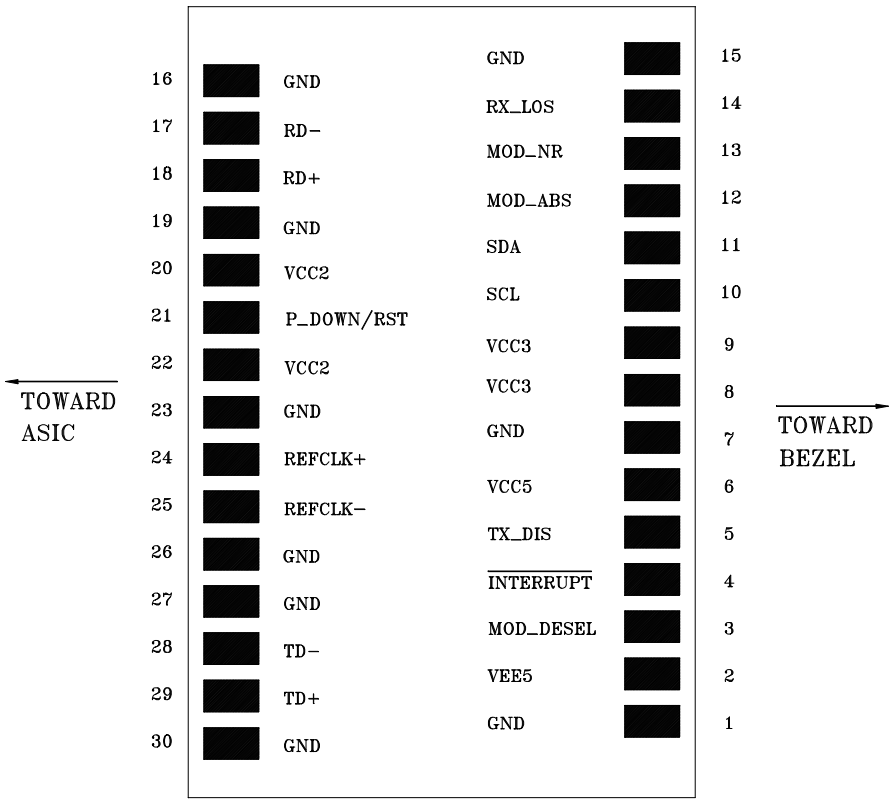


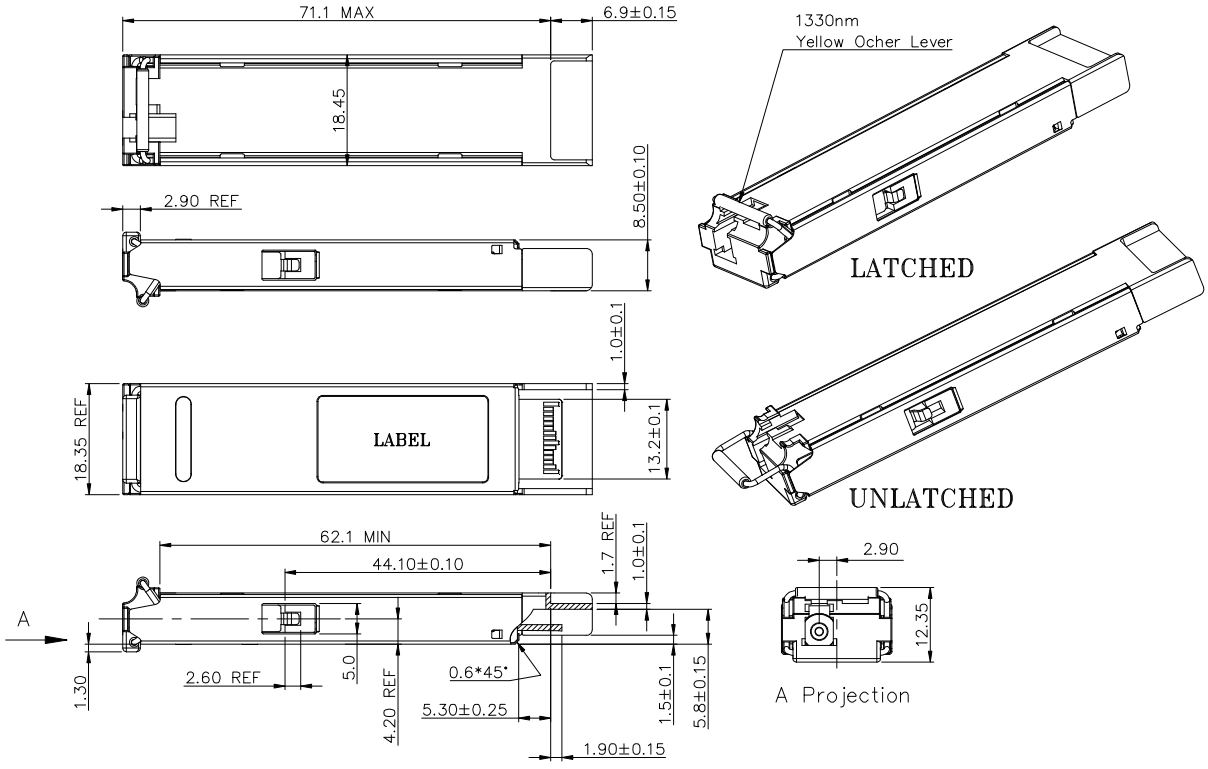
Table 3 PIN Description

PIN	Logic	Signal Name	Description	Note
1		GND	Module Ground	1
2		VEE5	-5.2V Power Supply **(Not required)**	3
3	LVTTL-I	Mod_Desel	Module De-select; When held low allows module to respond to 2-wire serial interface	
4	LVTTL-O	$\overline{\text{Interrupt}}$	$\overline{\text{Interrupt}}$; Indicates presence of an important condition which can be read over the 2wire serial interface	2
5	LVTTL-I	TX_DIS	Transmitter Disable; Turns off transmitter laser output	
6		VCC5	+5V Power Supply **(Not required)**	3
7		GND	Module Ground	1
8		VCC3	+3.3V Power Supply	
9		VCC3	+3.3V Power Supply	
10	LVTTL-I/O	SCL	Serial 2-wire interface clock	2
11	LVTTL-I/O	SDA	Serial 2-wire interface data line	2
12	LVTTL-O	Mod_Abs	Indicates Module is not present. Grounded in the Module	2
13	LVTTL-O	Mod_NR	Module Not Ready; Indicating Module Operational Fault	2
14	LVTTL-O	RX_LOS	Receiver Loss Of Signal Indicator	2
15		GND	Module Ground	1
16		GND	Module Ground	1
17	CML-O	RD-	Receiver Inverted Data Output	
18	CML-O	RD+	Receiver Non-Inverted Data Output	
19		GND	Module Ground	1
20		VCC2	+1.8V Power Supply **(Not required)**	3

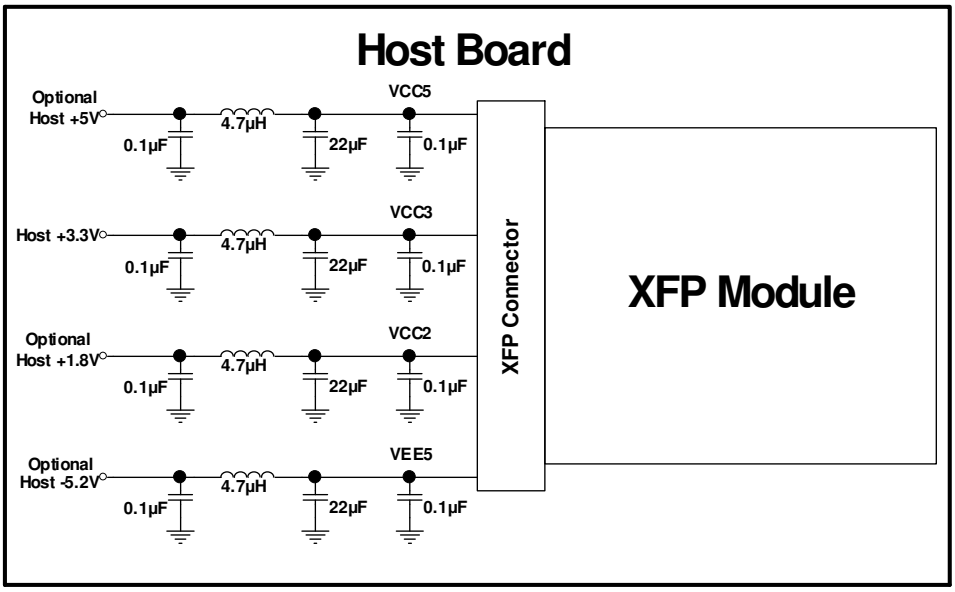
21	LVTTL-I	P_Down/RST	Power down; When high, requires the module to limit power consumption to 1.5W or below. 2-Wire serial interface must be functional in the low power mode.	
			Reset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.	
22		VCC2	+1.8V Power Supply **(Not required)**	3
23		GND	Module Ground	1
24	PECL-I	RefCLK+	Reference Clock Non-Inverted Input, AC coupled on the host board. **(Not used. Internally terminated to 50 ohm (100 ohm diff.))**	4
25	PECL-I	RefCLK-	Reference Clock Inverted Input, AC coupled on the host board. **(Not used. Internally terminated to 50 ohm (100 ohm diff.))**	4
26		GND	Module Ground	1
27		GND	Module Ground	1
28	CML-I	TD-	Transmitter Inverted Data Input	
29	CML-I	TD+	Transmitter Non-Inverted Data Input	
30		GND	Module Ground	1

1. Module ground pins GND are isolated from the module case and chassis ground within the module.
2. Shall be pulled up with 4.7K-10Kohms to a voltage between 3.15V and 3.45V on the host board.
3. These PINs are open within module.
4. A Reference Clock input is not required. If present, it will be ignored.

Mechanical Specification (Units in mm)



Recommended Power Circuit Schematic



Recommended Interface Circuit

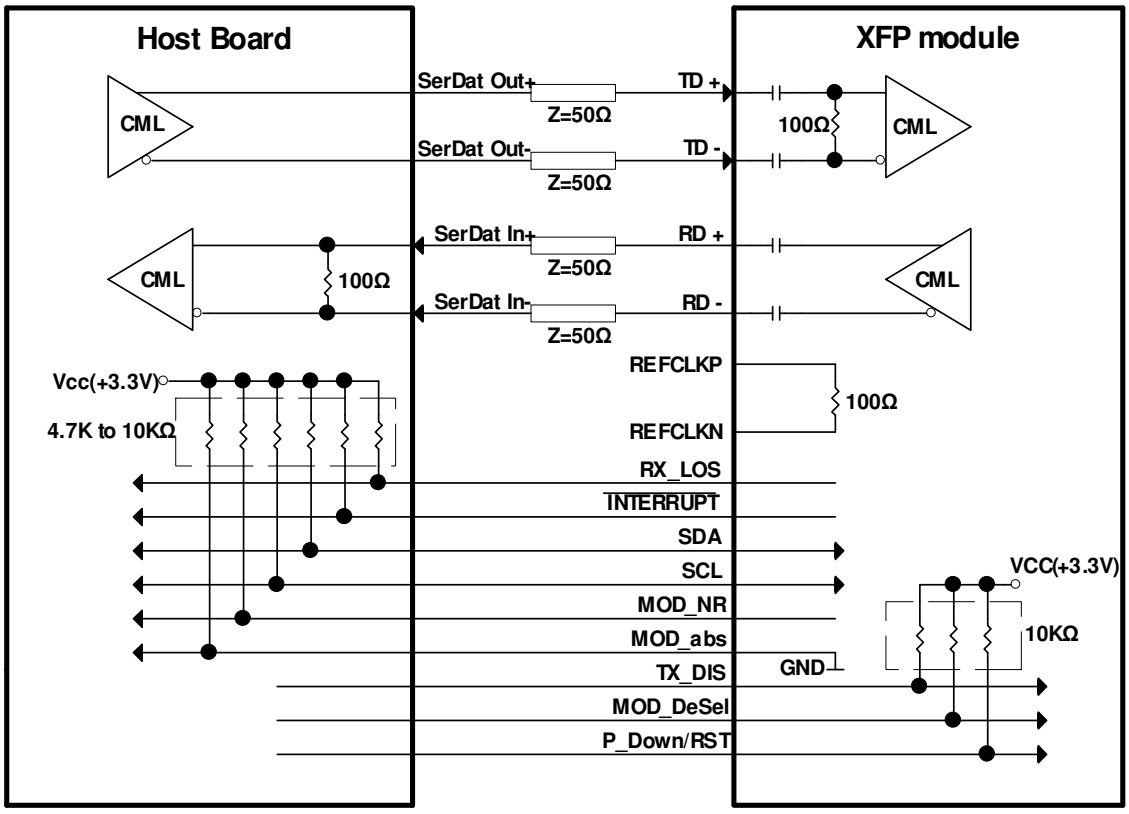


Table 2 Serial ID Memory Contents (Table 01h)

Address	Field Size (Byte)	Name of Filed	Description	Hex
128	1	Identifier	XFP	06
129	1	Ext. Identifier	power consumption <2 W, no Ref Clock required	50
130	1	Connector type	LC connector	07
131~138	8	Transceiver	8G FC 800-SM-LL-L	00 00 00 00 00 00 00 00
139	1	Encoding	8B10B, NRZ	50
140	1	BR-Min	1.063 Gbps	0A
141	1	BR-Max	8.5 Gbps	55
142	1	length (SMF)-Km	10 km	0A
143	1	Length (E-50µm)	0 m	00
144	1	Length (50 µm)	0 m	00
145	1	Length (62.5 µm)	0 m	00
146	1	Length (Copper)	0 m	00
147	1	Device Tech	Uncooled 1330DFB, PIN detector	40
148~163	16	Vendor name	OPTOWAY	4F 50 54 4F 57 41 59 20 20 20 20 20 20 20 20 20
164	1	CDR Support	CDR supports 8.5 ~ 1.063G, XFI Loopback	01
165~167	3	Vendor OUI		00 0E FA
168~183	16	Vendor PN	XPB-4910LWG	58 50 42 2D 34 39 31 30 4C 57 47 20 20 20 20 20
			XPB-4910BLWG	58 50 42 2D 34 39 31 30 42 4C 57 47 20 20 20 20
184~185	2	Vendor rev	ASCII (“31 61” means 1a revision)	xx xx
186~187	2	Wavelength	1330 nm	67 E8
188~189	2	Wavelength Tolerance	+/- 10nm	07 D0
190	1	Max Case Temp	70deg (for XPB-4910LWG)	46
			85deg (for XPB-4910BLWG)	55
191	1	CC_BASE	Check sum of Byte 128 -- 190	
192~195	4	Power Supply	2Wmax, 1.5W pd_max , 550mA 3.3V	64 96 06 00
196~211	16	Vendor SN	ASCII	xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx
212~219	8	Date code	ASCII Year (2 Byte), Month (2 Byte), Day (2 Byte)	xx xx xx xx xx xx 20 20
220	1	Diagnostic Monitoring Type	No BER Support, Average Power	08
221	1	Enhanced Options	Optional Soft TX_DISABLE implemented, Optional Soft P_down implemented	60
222	1	Aux Monitoring	AUX1 for Vcc3.	70
223	1	CC_EXT	Check sum of Byte 192 -- 222	
224~255	32	Vendor Specific		Reserved

Note: Specifications subject to change without notice.

REVISION HISTORY

Version	Subject	Release Date
1.0	Initial datasheet	2008/8/1
2.0	Revise package diagram	2017/10/12